

## CMOS Design of Focal Plane Programmable Array Processors

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**Abstract:** While digital processors can solve problems in most application areas, in some fields their capabilities are very limited. A typical example is vision. Simple animals outperform super-computers in the realization of basic vision tasks. The limitations of conventional digital systems in this field can be overcome following a fundamentally different approach based on architectures closer to nature solutions. Retinas, the front end of biological vision systems, obtain their high processing power from parallelism, and consist of concurrent spatial distributions (on the focal plane aerea) of photoreceptors and basic analog processors with local connectivity and moderate accuracy. This can be implemented using an architecture with the following main components are: a) parallel processing through an array of locally-connected analog processors; b) a means of storing, locally, pixel-by-pixel, the intermediate computation results, and 3) stored on-chip programmability. When implemented as a mixed-signal VLSI chip, devices are obtained which are capable of image processing at rates of trillions of operations per second with very small size and low power consumption. This paper reviews the latest results on this type of chips and systems, and outlines the envisaged roadmap for these computers.

### 1. Introduction

Conventional vision machines use a CCD camera for *parallel* acquisition of the input image, and *serial* transmission of a *digitized* version of the input data to a separate computer. This results in huge data rates which conventional computers can not analyze in real-time. For instance, a 3-color@512×512 camera delivers about  $F \times 10^6$  bytes/second, where  $F$  is the frame rate. Conventional computers and DSPs are able to manage such a huge rate for auto-focus, image stabilization, control of the luminance/chrominance, etc. However, executing the spatial-temporal operations of image processing in *real-time* requires much more sophisticated digital processors. Consequently, conventional vision machines with real-time capabilities are bulky, expensive and extremely power-hungry. This is in contrast to living beings, where even very tiny and power-efficient brains can analyze complex time-varying scenes in real-time. One of the keys to this high efficiency is the processing front-end of natural vision systems: the *retina* [1].

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This contrast between the performance of artificial and “natural” vision systems is, among other things, due to the inherent *parallelism* of the processing realized by the latter. Such parallelism is observed already in the retina [2]. It contains *photoreceptor cells* of two different types — called *cones* (about 6 million in the whole retina) and *rods* (about 120 million) — which perform a logarithmic three-color imaging for around ten decades of light intensity range. It also contains *processing cells* — called horizontal, bipolar, amacrine and ganglion cells — to perform non-linear spatial-temporal processing operations on the incoming flow of images through a sequence of layers. Among many other tasks, such processing serves to extract important features from the raw sensory data and, thus, to reduce the amount of information transmitted for subsequent processing [3][1].

Inspired by the efficiency of natural vision systems, universities and companies have focused their efforts on the development of new generations of devices capable of overcoming the drawbacks of traditional ones through the incorporation of distributed parallel processing, and by making this processing act concurrently with the acquisition of the signal. One possible strategy to achieve that is through flip-chip bonding of separate sensing and processing devices; another possibility is to incorporate the sensory and the processing circuitry on the same semiconductor substrate. “Silicon retinas”, “smart-pixel chips” and “focal-plane array-processors” are members of this latter class of vision chips [4][5][6]. Their development is expected to have a significant impact in quite diverse scenarios. However, industrial applications demand chips capable of flexible operation, with programmable features and standard interfacing to conventional equipment. A powerful methodological framework for a systematic development of these types of chips is using the paradigm of analogic cellular computing [7] [8].

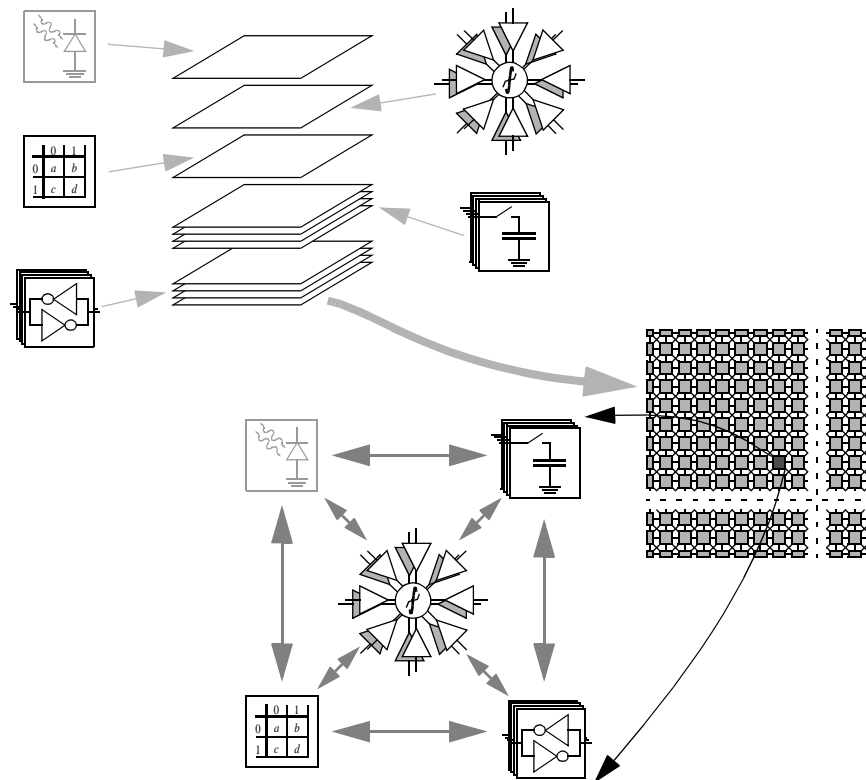
## 2. Description of the Architecture

Fig. 1 contains a conceptual architecture of programmable focal-plane processing systems. Each processing element performs the functions of sensing (photoreceptor), analog processing (essentially based on local convolutions), logic processing (boolean gate) and storing (gray-scale and black&white). The convolution parameters and logic gate can be programmed in a spatially-invariant form (same parameter values for all processors). This programmability, combined with the internal pixel-wide storage capability allows the realization of complex image processing algorithms.

The on-chip incorporation of some additional circuitry around the processors array provides easy digital control of the processing algorithms, execution steps, and data interchange.

## 3. Examples of Chip Implementations

During the last few years several cellular programmable array processing chips have been designed. Particularly, those having a size larger than  $10 \times 10$  and whose operation have been actually demonstrated through experimental evidence are found in [9]-[14]. Table 1 presents a summary of some features associated to these chips. Last row in this table refers to a new prototype, ACE16K, recently submitted to foundry.



**Fig. 1: Conceptual architecture of programmable focal-plane processing systems.**

Speed is expressed in terms of analog operations per second. The equivalent digital multiply/add operations per second can be calculated in such a way that 10 time steps are supposed in a time constant. This is a default needed when the A template is full and analog input or output values are present. This means  $10 \times 20 = 200$  equivalent multiply/add operations per time constant, so that calculating with 4096 cell processors and about 280ns time constant [14], the equivalent speed is about 3 TeraOPS.

The data in this table reveals a trade-off between speed and accuracy – common to any analog integrated circuit. Out from these chips, those reported in [11] [14] and ACE16K have embedded distributed optical sensors; i.e. they are true focal plane array processors. On the other hand, only ACE16K and that reported in [14] are capable to operate with gray scale inputs and producing gray outputs, while at the same time having all functional features stated in the Introduction.

The chip in [14] has served as a vehicle to demonstrate the concept of true VLSI analog chips with robust, controlled and predictable response. From here, basic challenges were to increase the size and to improve the I/O performance [15]. The new ACE16K prototype follows this trend.

The integration of multiple sensors per pixel within the array computer probably defines the dominant medium- and long-term scenario for systems based on these chips [16]. The multiple sensors should be adaptive and capture different modalities, spectra,

sensitivity and dynamics. Their control parameters should be set by underlying programmed calculations. Hence, the multi-sensor image acquisition depends, pixel by pixel, on the actual changing scene to be analyzed.

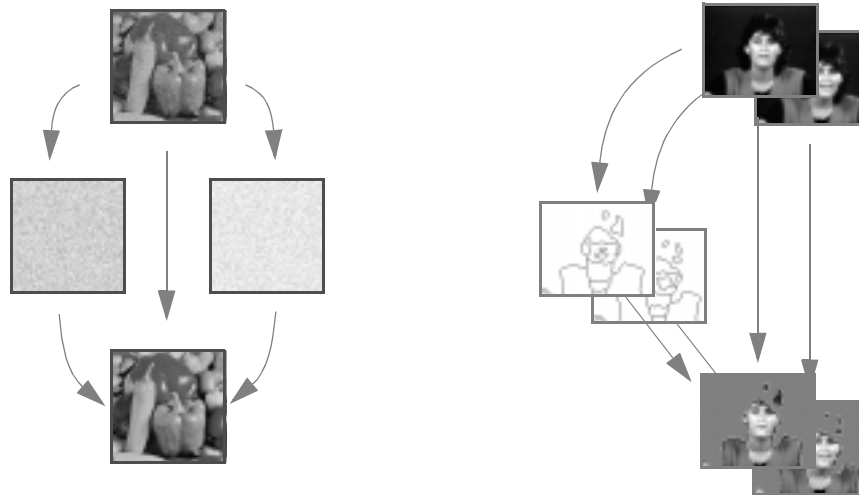
**Table 1: Summary and comparison of recent chip implementations**

Reference	Technology (CMOS ( $\mu\text{m}$ ))	Design Style <sup>a</sup>	Array Size (cells)	Die Size ( $\text{mm}^2$ )	Cells Density (cells/ $\text{mm}^2$ )	Speed XPS <sup>b</sup>	XPS/cell	XPS/ $\text{mm}^2$	XPS/ $\text{mW}$	Stored Program	Analog Resolution (eq. bits)	Optical Sensors	Electrical Input <sup>c</sup>	Electrical Output <sup>c</sup>	Embedded Images Memory	Digital External Control
[9]	1.0	MS	32 x 32	70	31	0.30T	0.30G	9.3G	---	✓	6-7		A	B	✓	✓
[10] <sup>d</sup>	0.7	A	20 x 20	25	17	12.5G	31M	0.52G	82M		6-7		A	B		
[11]	0.8	MS	20 x 22	30	28	0.13T	0.30G	8.25G	0.12G	✓	6-7	✓	B	B		✓
[12]	0.5	BD	48 x 48	11.4	295	7.65T	3.76G	1.11T	25G	✓	2		B	B		✓
[13]	0.8	A	14 x 14	26	16	0.37T	1.89G	31G	1.24G		4		A	A		
[14] <sup>e</sup>	0.5	MS	64 x 64	87	81	0.40T	98M	7.93G	0.33G	✓	7-8	✓	A + B	A + B	✓	✓
.. <sup>f</sup>	0.35	MS	128 x 128	130	180	1.64T <sup>g</sup>	100M <sup>g</sup>	18G <sup>g</sup>	---	✓	7-8	✓	D	D	✓	✓

- a. MS: Mixed-Signal, A: Analog, BD: Basically Digital
- b. XPS: Analog Operations Per Second, is an equivalent measurement indicating the number of analog arithmetic operations like addition, subtraction, multiplication and division.
- c. A: Analog, B: Binary, D: Digital (digitalized gray-scale).
- d. The convolutors in this chip have vertical and horizontal interconnections, but not diagonals.
- e. Some additional functionalities of this design include: local evolution enabling mask, global binary gates for fast binary output-images evaluation, cyclic spatial boundary conditions.
- f. Design presently in foundry. This chip has some additional functionalities: full digital interface (control and data), synchronous address event output for sparse binary images, local data-transference and evolution enabling masks, selectable linear-logarithmic photoreception.
- g. Preliminary data from simulations.

#### 4. Application Algorithms: Some Examples

Fig. 2 illustrates two application examples, namely nonlinear impulse-noise removal and real-time image segmentation, taken from those demonstrated by the chip referred in [14]. Further applications and results are described in the DICTAM project web page <http://www.imse.cnm.es/~dictam>.



**Fig. 2: Application examples: a) non-linear salt&pepper noise removal, b) real-time image segmentation.**

#### 5. Prospects for Future Developments and Applications

The exploitation of higher resolution technologies will certainly allow the production programmable focal-plane array processors with array sizes in the range of 256 x 256 and beyond. Even with present resolutions (128 x 128), the application scope and possible tasks for this type of systems include key areas like

image segmentation, pattern recognition, objects classification, object counting, motion detection and estimation, activity detection, attention triggering and orientation, high speed search of relevant sectors in large images, image fusion, path finding, real-time spatio-temporal linear/nonlinear image filtering, artificial vision tasks, early vision., image processing front-ends, tracking, surveillance, real time video compression, intelligent toys, quality control systems, multimedia applications, teleconferencing, videophony, defense systems, and medical imaging.

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